IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A computer system comprising:

at least one processor;

an identification signal detection circuit for receiving a wireless identification signal from an identification object, the wireless identification signal containing identification information regarding the assigned processor of the identification object;

a memory having means for determining whether the assigned processor of the identification object as indicated by the wireless identification signal has authorized access to computer information accessible by the computer system; and

~~a memory having means for determining that the identification signal detection circuit has not received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access~~

a memory having means for placing the computer system in a condition to deny access by placing the computer system in a lower power state in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

2. (Original) The computer system of claim 1 further comprising:

a memory circuit programmable to store a list of at least one user having authorized access to computer information assessable by the computer system.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The computer system of claim ~~3~~ 1 wherein placing the computer system in a condition to deny further includes logging a user off of the computer system in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

6. (Currently Amended) The computer system of claim ~~3~~ 1 wherein placing the computer system in a condition to deny further includes placing the computer system in a locked state in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

7. (Currently Amended) The computer system of claim ~~3~~ 1 further comprising:

a memory circuit storing operating system code whose execution by the at least one processor implements an operating system for controlling the operation of the computer system; and

wherein the operating system code includes code whose execution places the computer system in a condition to deny access to computer information accessible by the computer system in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

8. (Original) The computer system of claim 1 wherein the identification signal detection circuit further includes:

a controller operably coupled to the memory having means for determining whether the assigned possessor of the security object and operably coupled to the memory having means for determining that the identification signal detection circuit has not received for a predetermined period of time.

9. (Original) The computer system of claim 1 wherein the identification signal detection circuit, the memory having means for determining whether the assigned possessor, and the memory having means for determining that the identification signal detection circuit has not received are implemented on a computer add in card.

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10. (Original) The computer system of claim 1 wherein:

the memory having means for determining that the identification signal detection circuit has not received for a predetermined period of time is implemented in the identification signal detection circuit; and

the identification signal detection circuit provides a signal in response to a determination that the identification signal detection circuit has not received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

11. (Original) The computer system of claim 10 wherein the identification signal detection circuit generates an interrupt in response to a determination that the identification signal detection circuit has not received for a predetermined period of time.

12. (Original) The computer system of claim 10 wherein the identification signal detection circuit asserts a #PME signal in response to a determination that the

identification signal detection circuit has not received for a predetermined period of time.

13. (Original) The computer system of claim 12 further comprising:

a chipset circuit having an input to receive the #PME signal from the identification signal detection circuit.

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14. (Original) The computer system of claim 1 wherein the memory having means for determining whether the assigned possessor of the security object and the memory having means for determining that the identification signal detection circuit has not received for a predetermined period of time, are both implemented in the same memory circuit of the identification circuit.

15. (Original) The computer system of claim 1 wherein the identification signal detection circuit is operably coupled to the processor via a power managed computer bus.

16. (Previously Amended) The computer system of claim 1 wherein:

the identification signal detection circuit has an output to provide an indication signal indicating that the identification signal detection circuit has received a wireless identification signal containing identification information of an assigned possessor of a security object determined to have authorized access; and

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wherein the identification signal is provided in response to receiving a wireless identification signal containing identification information of an assigned possessor of a security object determined to have authorized access after a predetermined period of time of not receiving an identification signal containing identification information of an assigned possessor of a security object determined to have authorized access.

17. (Original) The computer system of claim 16 wherein:

the identification signal detection circuit is operably coupled to the at least one processor via a computer bus substantially conforming to a PCI Local Bus Specification; and

the indication signal includes an assertion of the #PME signal.

18. (Original) The computer system of claim 1 further comprising:

a memory having means for placing the computer system in a higher power state from a lower power state if it is determined that the identification signal detection circuit has received a wireless identification signal containing identification information of an assigned possessor having authorized access.

19. (Previously Amended) The computer system of claim 1 further comprising:

a memory having means for implementing a state machine including at least one state of a first state type and at least one state of a second state type;

wherein in a state of the first state type, the identification signal detection circuit is receiving identification signal containing identification information of an assigned possessor having authorized access within a predetermined period of time from a previously received identification signal containing identification information of the assigned possessor having authorized access; and

wherein in state of the second state type, the identification signal detection circuit is not receiving an identification signal containing identification information of an assigned possessor having authorized access within a predetermined period of time from a previously received identification signal containing identification information of the assigned possessor having authorized access.

20. (Original) The computer system of claim 19 wherein the identification signal detection circuit further includes:

a controller operably coupled to the memory having means for implementing a state machine, the state machine being implemented by the controller.

21. (Currently Amended) A method for controlling access to computer information comprising:

sending a wireless identification signal by an identification object, the wireless identification signal including identification information regarding an assigned possessor of the object;

receiving, independent of a conscious access action by a user, the wireless identification signal by a detection circuit;

determining whether the assigned possessor as indicated by the wireless identification signal has authorized access to computer information accessible by a computer system; ~~and~~

granting access to computer information accessible by the computer system if it is determined that the assigned possessor as indicated by the wireless identification signal is authorized access, wherein the granting access to computer information accessible by the computer system further includes placing the computer system in a higher power state from a lower power state; and

denying access to computer information accessible by the computer system by placing the computer system in the lower power state if the computer system has not received for a predetermined period of time, a wireless identification signal containing identification information from an assigned possessor having authorized access.

22. (Original) The method of claim 21 wherein sending the wireless identification signal includes implementing a shaped binary frequency modulated signal.

23. (Original) The method of claim 21 wherein the identification object includes an identification badge and a transmitter circuit embedded in the badge.

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24. (Original) The method of claim 21 wherein the determining whether the assigned possessor is authorized access further includes:

determining by the execution of code whether an indication of the assigned possessor is included in a preprogrammed computer readable list of indications of users having authorized access.

25. (Original) The method of claim 21 wherein the execution of code is performed by a controller of the detection circuit.

26. (Canceled)

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27. (Original) The method of claim 21 wherein the granting access to computer information assessable by the computer system further includes placing the computer system in an unlocked state.

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28. (Previously Amended) The method of claim 21 wherein the granting access further includes:

displaying on a user interface a message requesting a user to provide a password;

determining whether the password provided by the user is assigned to the assigned possessor determined to have authorized access; and

granting access to computer information assessable by the computer system if determined that the password is assigned to the assigned possessor.

29. (Original) The method of claim 21 further comprising:

denying access to computer information accessible by the computer system in response to a determination that the detection circuit has not received for a predetermined period of time, a wireless identification signal including information regarding an assigned possessor having authorized access.

30. (Original) The method of claim 29 wherein denying access further includes placing the computer system in a locked state from an unlocked state in response to a determination that the detection circuit has not received for a predetermined period of time, a wireless identification signal including information regarding an assigned possessor having authorized access.

31. (Original) The method of claim 29 wherein denying access further includes logging a user off of the computer system in response to a determination that the detection circuit has not received for a predetermined period of time, a wireless identification signal including information regarding an assigned possessor having authorized access.

32. (Original) The method of claim 21 further comprising:

providing a signal by the detection circuit that the detection circuit has not received for a predetermined period of time, a wireless identification signal including information regarding an assigned possessor having authorized access.

33. (Original) The method of claim 32 wherein the providing the signal includes generating an interrupt.

34. (Original) The method of claim 32 wherein the providing the signal includes asserting a #PME signal.

35. (Previously Amended) An identification object for an assigned possessor comprising:

a circuit including:

a controller;

an antenna; and

a memory operably coupled to the connector, the memory having means for generating an information signal periodically broadcast via the antenna, the information signal containing identification information regarding the assigned possessor.

36. (Original) The identification object of claim 35 wherein the identification object is implemented as a security badge.

37. (Original) The identification object of claim 35 wherein the signal is broadcast range of at least ten feet.